Adiabatic Electrode Stimulator

55

Shawn K. Kelly

Contents

Abstract

This chapter discusses neural stimulator circuits, focusing on the power consumed in such circuits. The basis of neural communication, the action potential, involves the movement of ions across the nerve membrane, and externally applied electrical currents create electric fields that can modulate that ion movement to induce action potentials. These currents are generally applied by

S. K. Kelly (✉)
VA Pittsburgh Healthcare System, Pittsburgh, PA, USA

Institute for Complex Engineered Systems, Carnegie Mellon University, Pittsburgh, PA, USA
e-mail: skkelly@cmu.edu

M. Sawan (ed.), *Handbook of Biochips*,
https://doi.org/10.1007/978-1-4614-3447-4_19

a pulsed current source circuit, but these circuits waste a large amount of electrical power. An architecture is put forth here that uses a series of stepped voltage sources to drive charge onto an electrode in a manner similar to that used in adiabatic digital circuits. A sample system is described that creates five voltage supplies on capacitors from a single secondary telemetry coil voltage. Test results from this system show a power reduction of 53 % compared to a current source using the same chip voltage supplies and a power reduction of 66 % compared to a current source using the lowest reported voltage supplies for the same type of electrode.

Introduction

Neural tissue is stimulated for a number of purposes, from neuromodulators to treat Parkinson's disease or chronic pain (Testerman et al. 2006) to neural prostheses to restore hearing to the deaf (Hallum et al. 2007) or sight to the blind (Kelly et al. 2011). While the introduction of electrical current to create or modulate neural activity can have many beneficial effects, it can also have negative effects. Too much electrical power consumption can increase the temperature of surrounding tissue, causing damage (Gosalia et al. 2004). In addition, a larger power requirement for the implant exposes the patient to larger magnetic fields from the inductive wireless transfer used in many implantable devices. For devices with an implanted battery, excessive stimulation power consumption will reduce the life of the battery and increase the frequency of surgery to change the device. For a number of reasons, it is beneficial for a designer to reduce the power consumed by a neural stimulator circuit.

One example of a neural prosthesis is the retinal implant for the blind. This device, shown in Fig. 1, restores some useful sight to patients blind with

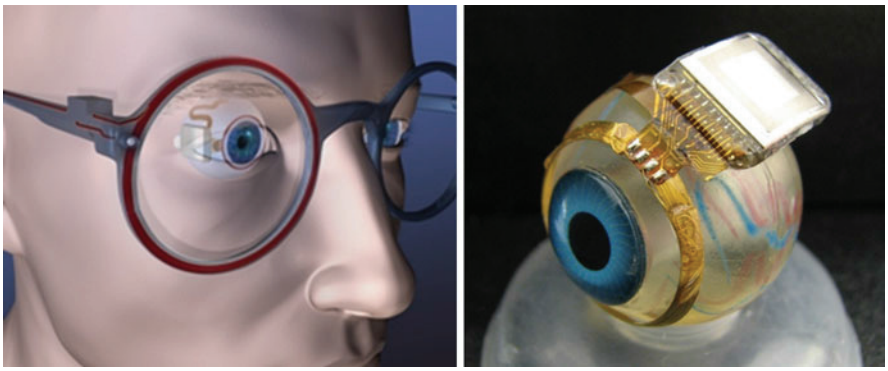

Fig. 1 The retinal prosthesis for the blind. *Left* – A retinal prosthesis as conceptualized, showing the small camera and coil for power and data telemetry mounted in the glass frame, as well as the implant attached to the eye. *Right* – An early prototype of the retinal prosthesis attached to a model eye

degenerative retinal diseases. Images are captured by a camera mounted on glasses and processed by a cell phone-sized computer. The processed image data are wirelessly transmitted to the implanted device, which in turn stimulates retinal ganglion cells to create a pixelated form of the image. Results with lower-channel-count devices have shown some promise (Humayun et al. 2012), and researchers are pushing to develop retinal prostheses with greater numbers of independent stimulating channels (Chen et al. 2013; Kelly et al. 2013). There are several reasons why stimulation power consumption is a concern in a retinal prosthesis. (1) The prosthesis receives wireless inductive power transfer from an external battery, (2) it has a very large number of independent stimulation channels, and (3) the stimulating electrode is located in the retinal tissue, which is particularly susceptible to temperature-induced damage.

Power is consumed in the tissue and the electrode, in the circuits that create the stimulus current, and in any coils and circuits that transfer power to the implant from an outside battery. The power consumed in the tissue and electrode is generally considered to be useful power to induce neural action potentials and is influenced by parameters of the stimulus pulses, as well as a number of physical properties of the electrodes, neurons, and surrounding tissue, as described in section "Electrical Stimulation of Neural Tissue." The power consumed in the coils and power transfer circuits can be optimized in a number of ways not addressed here. The power consumed in the circuits that generate the neural stimulus, however, is largely waste power that contributes to tissue heating. Methods of reducing the circuit power are explored in this chapter, including an architecture that uses the principles of adiabatic digital circuits to minimize power consumption.

Electrical Stimulation of Neural Tissue

Minimization of stimulation power requires an understanding of the physics of electrical neural stimulation. Neural cells create action potentials by modulating the flow of ions, primarily sodium (Na^+) and potassium (K^+), into and out of the cells along their concentration gradients (Weiss 1996). An action potential can be externally induced by applying an electrical current.

It is well understood that a nerve's cell membrane can be modeled by a capacitor with several voltage-dependent ion conductance paths in parallel, as shown in Fig. 2. At rest, the inside of a typical nerve cell is approximately −60 mV with respect to the outside. Depolarizing the membrane voltage from rest to make it more positive will cause a sharp increase in the sodium conductance. More sodium ions then flow into the cell, driving the internal voltage more positive, further increasing the sodium conductance. This positive feedback loop rapidly drives the cell potential toward the positive sodium Nernst potential that balances the sodium ion concentration, creating the action potential.

Membrane depolarization is caused by a current flowing out of the cell, creating a positive charge on the inside of the membrane capacitance. This outward membrane current is induced by the second spatial derivative of voltage along the axon,

called the activating function (Weiss 1996). In Eq. 1, V_m is the membrane potential, z is the axis along the length of the nerve's axon, K_m is the membrane current per unit length, and r_o and r_i are the external and internal resistances per unit length, respectively.

$$\frac{\partial^2 V_m}{\partial z^2} = (r_o + r_i)K_m \tag{1}$$

Electrical stimulation is generally delivered by a negative pulse of constant current through an electrode near the axon. The stimulating pulse is generally followed by a pulse of positive current to balance the delivered charge and prevent long-term reduction and oxidation reactions at the electrode-tissue interface. A brief delay between the pulses reduces stimulation thresholds by delaying the hyperpolarizing current and also allows examination of the electrode-tissue interface voltage (Gorman and Mortimer 1983). This delay will be eliminated from the discussion going forward to simplify the argument. Typical biphasic current pulse waveforms are shown in Fig. 3.

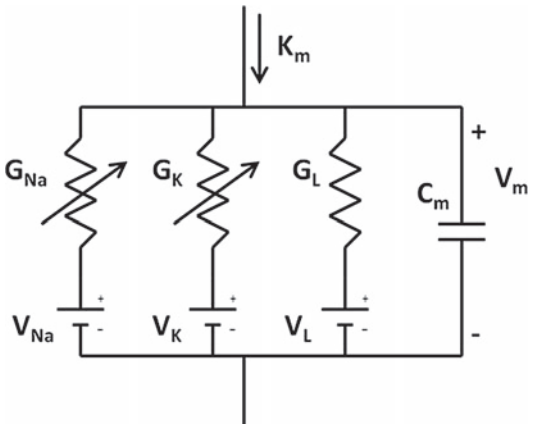

Fig. 2 Nerve membrane model showing the membrane capacitance; ion conductances; Nernst potentials for sodium, potassium, and all other ions (leakage current); and the membrane current and voltage

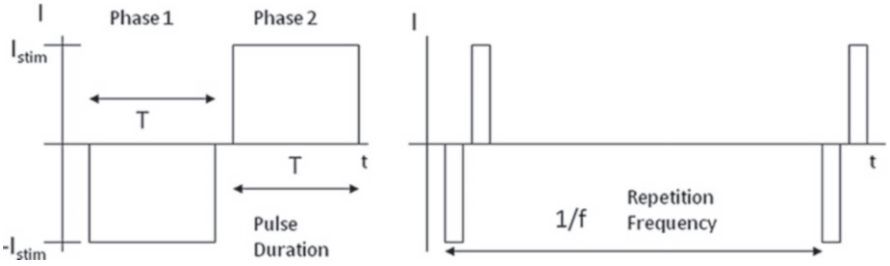

Fig. 3 Typical balanced biphasic current stimulation pulses. The negative (cathodic) phase induces an action potential in the nerve, while the positive (anodic) phase balances the charge through the electrode. Biphasic pulses are repeated at a regular frequency

The negative current flowing from the electrode creates a voltage throughout the tissue. Imagine a small spherical stimulating electrode sitting a distance x from an axon, with a large return electrode far away. The potential at a distance r from the stimulating electrode is:

$$V(r) = \frac{\rho I}{4\pi r} \tag{2}$$

However, for the axon sitting a distance x away from the electrode, the voltage along its z direction is:

$$V(z) = \frac{\rho I}{4\pi\sqrt{x^2 + z^2}} \tag{3}$$

The activating function is the second derivative with respect to z along the axon:

$$\frac{\partial^2 V}{\partial z^2} = \frac{\rho I}{4\pi} \frac{2z^2 - x^2}{(x^2 + z^2)^{5/2}} \tag{4}$$

Though this expression appears complicated, the normalized function is visualized graphically in Fig. 4 for a negative current pulse. Note that the second derivative, the activating function, has a large positive region in the center with

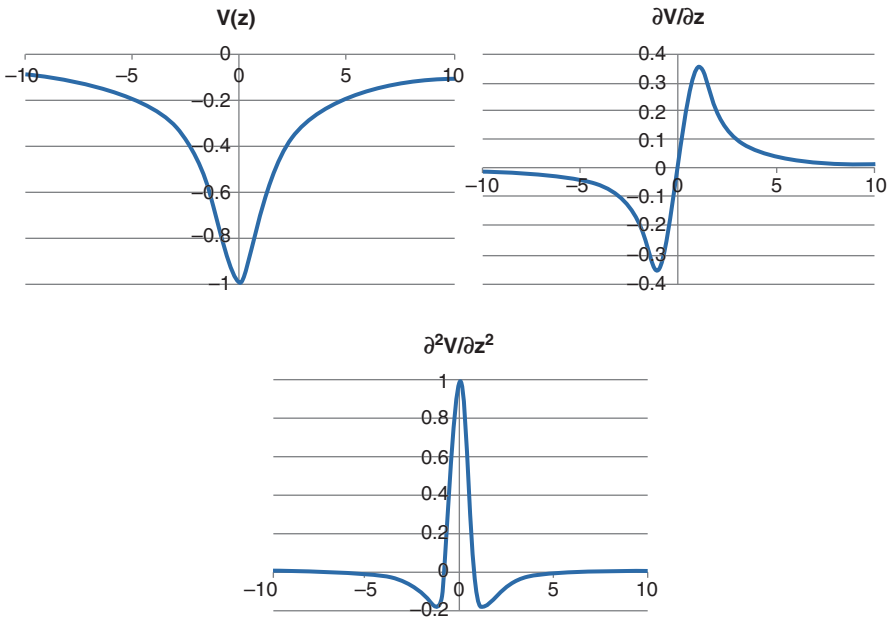

Fig. 4 Normalized voltage along the z direction of the axon, along with its first and second derivatives

negative lobes. From Eq. 1, this means that an outward, depolarizing current occurs nearest the stimulating electrode, and smaller inward, hyperpolarizing currents occur on either side. From Eq. 4, it is clear that the activating function is increased as x decreases. In other words, moving the electrode nearer to the axon increases the effectiveness of electrical stimulation, decreasing the current, and therefore the power, required.

The threshold current required to stimulate a nerve is determined experimentally and is often plotted against the duration of the current pulse in a strength-duration plot. These data have been modeled by Eq. 5, where T is the width of the negative current phase, τ is the nerve membrane time constant, and I_{Rh} is the rheobase current, the minimum current required to induce an action potential at any phase width (Lapicque 1907). For a modest range of phase duration values, the threshold can be approximately modeled as a constant stimulus charge. For much longer phase durations, the threshold approximates a constant current.

$$I_{th} = \frac{I_{Rh}}{(1 - e^{-T/\tau})} \tag{5}$$

Figure 5 shows plots of strength-duration $I(T)$, charge-duration $Q(T)$, and power-duration $P(T)$ for threshold stimulation through an electrode near an axon. The power-duration curve shows the average power consumed in an electrode, modeled

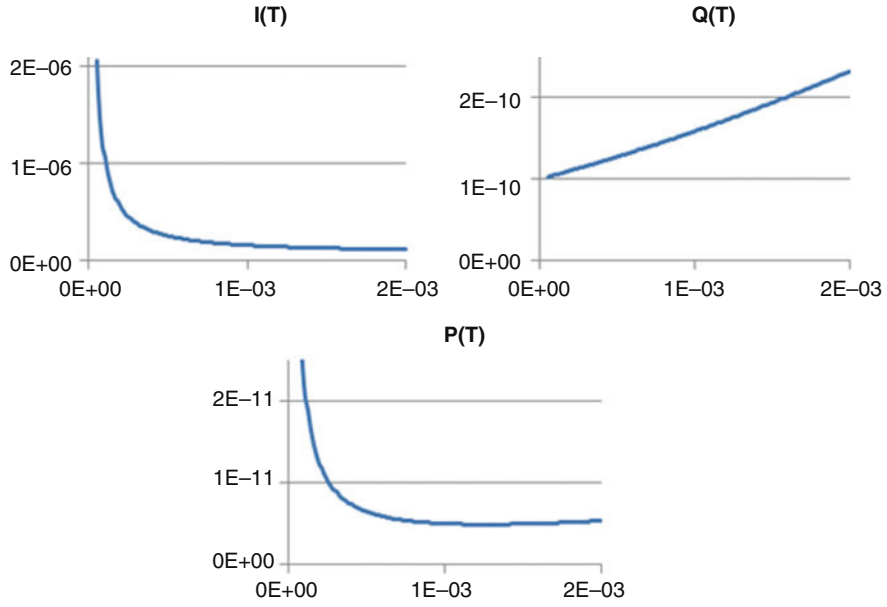

Fig. 5 Strength-duration curve showing threshold current vs. pulse duration, along with charge-duration curve and power-duration curve

here as a series resistance R and capacitance C, while driving stimulus current through it at a typical repetition frequency f. The factor of two in Eq. 6 accounts for the two current phases in the biphasic stimulus pulse.

$$P(T) = 2I^2RTf \tag{6}$$

Note that the power-duration curve shows a phase width at which there is minimum power consumption within the electrode. This power consumption will be explored further in section "Electrode-Tissue Interface."

Electrode-Tissue Interface

The interface between the electrode and the tissue will be examined for two reasons. Our understanding of the electrode impedance can be used both to calculate the amount of useful power needed within the electrode for nerve stimulation and to design circuits that are less wasteful when delivering stimulus current to the tissue. There are a variety of electrode impedance models used for different purposes.

There are two portions of a typical electrode model, one modeling the resistive current path through the tissue and any resistive paths through the electrode, and one modeling the interface between the electrode and the tissue. Since metals conduct electricity with electrons and tissue fluids conduct electricity with ions, the interface must include some interaction between those carriers. The two ways which will be discussed in this section are capacitive coupling and reduction and oxidation reactions.

A simple electrode model, one often used to calculate electrode voltage requirements and power consumption, is a series resistor and capacitor. The capacitor represents the charge boundary layer at the metal-fluid interface and the oxidation state change of electrode metals, while the resistor represents the fluid resistance and the access resistance of the electrode. Since the electrodes are typically driven by a charge-balanced, biphasic constant current pulse, as was shown in Fig. 3, the resulting voltage across the electrode resistance and capacitance is the step-ramp waveform that is shown below in Fig. 6.

More complex electrode models generally use some form of conductance, in parallel with the metal-fluid interface capacitor, to represent reduction and oxidation reactions. Some models include a constant phase element or Warburg impedance (Merrill 2010). The parallel conductance path, not shown in Fig. 6, will curve the ramping portion of the waveform slightly. Additionally, there is usually a soft corner on the transition from the step to the ramp due to the distributed resistance-capacitance at the interface and nonlinearities of the electrode impedance. Circuits that roughly approximate the electrode voltage waveform will be designed, so a simple resistor-capacitor model is sufficient for our purposes.

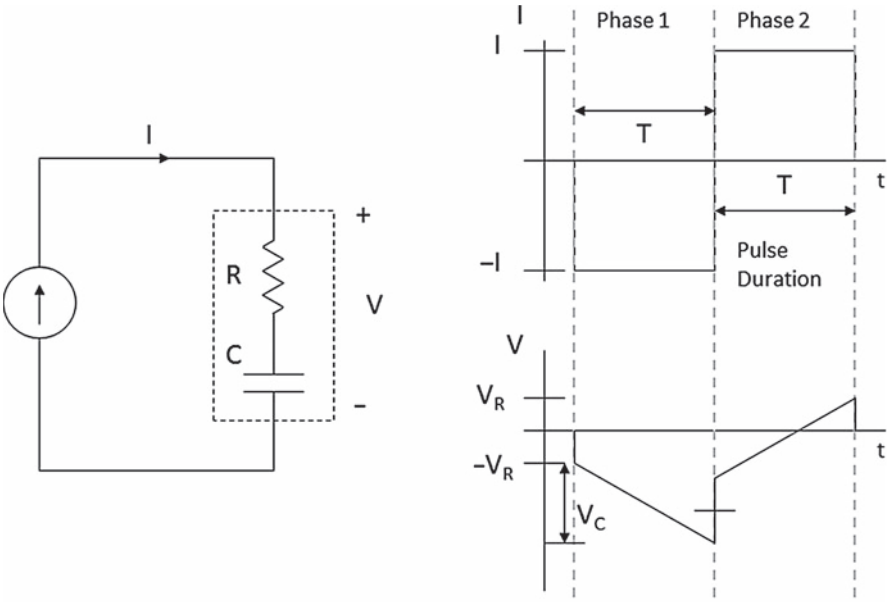

Fig. 6 Electrode voltage waveform in response to a biphasic current stimulus. The step results from the pulse of current through the resistance, and the ramp is the integration of constant current on the capacitance

Power Consumption in Traditional Neural Stimulators

Using the simple series RC model for an electrode, the instantaneous power consumed within the electrode while stimulus current is flowing through it is simply I^2R. The average power consumption was given in Eq. 6 above, but can be recast as:

$$P(T) = \frac{2Q^2Rf}{T} \tag{7}$$

This equation assumes that, to first order, the threshold for a given electrode-tissue configuration across a modest range of phase durations is a constant charge. Note that the capacitance does not factor into the power consumed within the electrode, since capacitors merely store energy and do not consume it (fCV^2 power in a digital circuit is consumed by the resistances associated with the transistors, not by the capacitance). One lesson to be extracted from Eq. 7 is that, for constant threshold charge, electrode resistance, and repetition frequency, the power consumed within the electrode depends only on pulse duration, and longer durations of stimulation at lower currents reduce the power consumption. This duration is subject to biological constraints, engineering constraints, and the constraint that the constant threshold charge assumption remains valid. Furthermore, different stimulation current pulse durations may generate qualitatively different responses in neural tissue (Fried

et al. 2006; Jensen et al. 2005). Another lesson that can be learned from this equation is that the power consumed within an electrode is quite low. For 400 μm diameter thin-film planar electrodes placed relatively close to the tissue, typical parameter values might be $Q = 100$ nC, $R = 2$ KΩ, $f = 100$ Hz, and $T = 1$ ms, giving an average power consumption of 4 μW per electrode. As it will be soon discovered, this is far lower than the power consumed elsewhere in a typical stimulator circuit.

Equation 7 shows the power consumed within an electrode itself, but the majority of power consumption for a typical neurostimulator occurs instead within the circuitry. A typical type of current source works by connecting the electrode to a voltage supply through a transistor, which acts as a large variable series resistor to limit the current. The instantaneous power consumption is simply the product of the current and the supply voltage and is otherwise independent of current source design. Delivering the same 100 nC as described above, as 100 μA for 1 ms, from ±2.5 V supplies, results in 25 μW average system power consumption per electrode. The difference between this system power consumption and the 4 μW electrode power consumption is primarily attributed to the current source transistors.

Despite the energy inefficiency, there are nonetheless a number of benefits to this traditional current source design. The higher supply voltage leaves room for more linear current sources or cascode circuits. It also allows for shorter duration pulses of higher current, which may be desired in some cases, such as selectively stimulating retinal ganglion nerve cells rather than retinal bipolar cells. In addition, the higher voltage supply allows for substantial variation in the load impedance, as might occur with tissue growth over the electrodes. These benefits permit the current source to maintain constant current during a variety of stimulation pulses, but the quality of the constant current pulse may be less valuable in some applications than a reduction in power consumption. In the following section, methods of trading off current source performance for power reduction will be explored.

Reducing Sources of Loss

Electrode current and voltage waveforms have been examined in Fig. 6; now, the electrode power waveform, the product of the voltage and the current, will be explored. The shaded area on the left side of Fig. 7 is the energy stored in the electrode capacitance. Since this capacitive energy is returned in the second phase, the average of the whole power waveform is I^2R, as shown. Note that at the beginning of the second phase, the power delivered to the electrode is negative. During this time, the electrode in this example is sourcing power from its capacitance. On the right side of Fig. 7, the same waveform is shown, but with the power supplied by the current source shown as a straight line across the top. The shaded area represents the wasted power burned in the current source transistors.

Reducing Excess Voltage Drops

The wasted power in Fig. 7 can be reduced somewhat by simply lowering the voltage supplies from which the current is drawn, resulting in the power shown in Fig. 8. With lower currents delivered over longer pulse widths, as recommended in section "Power Consumption in Traditional Neural Stimulators" above, this supply voltage can be made quite low. The complication is that the voltage compliance requirements vary with electrode impedance and drive current, so that the voltage supply must be variable, in contrast to the traditional current source design. In addition, if the voltage compliance is reduced too far, the voltage supplies may not support the analog and digital control and communication circuitry required for the

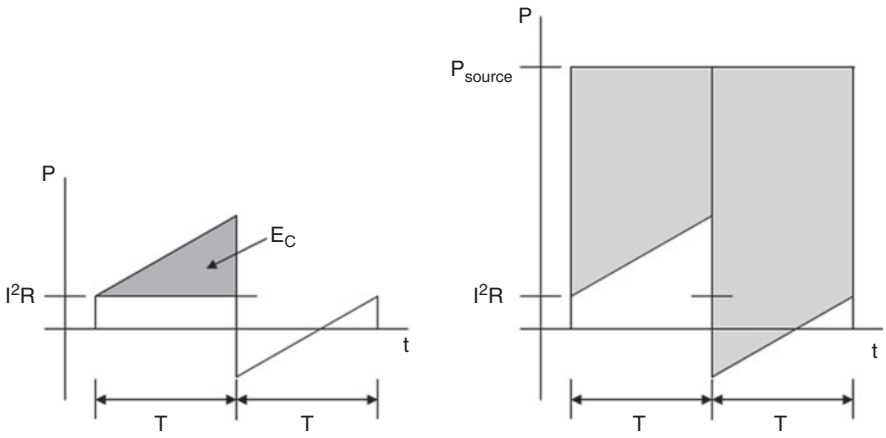

Fig. 7 Electrode power consumption and current source power. *Left*, power delivered to the electrode, with the capacitive stored energy shown in the shaded region. *Right*, power supplied by a traditional current source, with the wasted power shown in the shaded region

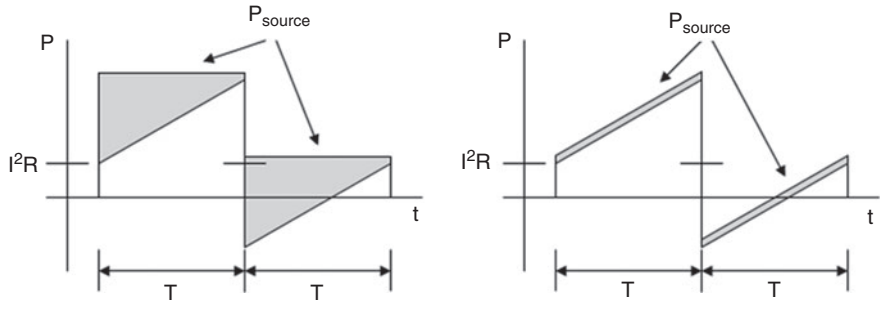

Fig. 8 Current source power consumption. *Left*, power supplied by a current source with reduced voltage supplies, with the wasted power shaded. *Right*, power supplied by a nearly ideal source with nearly zero voltage drop above the electrode voltage

implant. Thus, this method of power reduction may require separate, independent voltage supplies. The constant, higher voltage control circuitry supply may be generated simply from the receiver coil with diodes. The variable, lower voltage supply must be generated by some sort of efficient active rectification or power conversion. Work has been done on efficient DC-DC converters and active synchronous rectifiers (Pan et al. 1999; Jia et al. 2008), but most of these circuits are designed for high-power applications. A solution that uses very little overhead power and no additional inductors will be preferred, due to space constraints in a biomedical application.

Reducing Excess Voltage Drops

To eliminate the remaining shaded triangles in the left portion of Fig. 8, a current source can be conceived whose voltage tracks the voltage on the electrode. This current source would have virtually no wasted power dissipation, as shown in the right portion of Fig. 8. As before, note that in the beginning of the second phase in Fig. 8, the electrode capacitance is returning power to the current source. During this time, the stimulator is recovering power from the electrode, and, specifically, during the second phase shown in the right portion of Fig. 8, the stimulator recovers net *energy* from the electrode.

This power and energy recovery does not always take place, depending on the ratio of the electrode *RC* time constant to the pulse duration. Figure 9 shows example power waveforms. The left waveform shows power recovery at the beginning of the second phase, but zero net second-phase energy recovery. This occurs when the maximum voltage across the capacitor is twice the voltage across the resistor, or:

$$\begin{aligned} \frac{IT}{C} &= 2IR \\ RC &= \frac{T}{2}. \end{aligned} \tag{8}$$

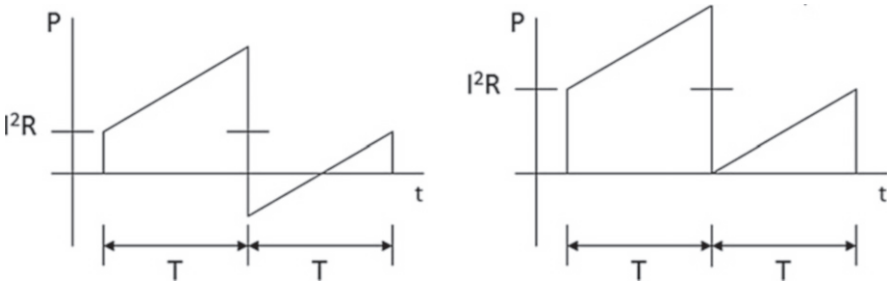

Fig. 9 Sample power waveforms. *Left*, power is recovered in the first half of the second phase, but no net energy is recovered. *Right*, no power is recovered during the second phase

The right side of Fig. 9 shows a case in which no power is ever recovered from the electrode. This occurs when the maximum capacitive voltage and the resistive voltage are equal, or:

$$RC = T. \tag{9}$$

Approximate Voltage Waveform

The step-ramp waveform created by a biphasic constant current source has been seen in Fig. 6, and it was learned that reducing the voltage overhead in any current supply circuits will reduce the power consumed by the circuitry. The ramping voltage supply shown in the right side of Fig. 8 would seem to be the optimal way to supply current to an electrode, but an alternative, and more easily realizable, architecture is one that approximates the step-ramp electrode waveform with a series of voltage steps (Kelly and Wyatt 2011). Figure 10 again shows the electrode current and voltage waveforms along with the voltage step stimulator architecture. This implementation is similar in some ways to the adiabatic circuits used to reduce power in digital design (Dickinson and Denker 1994; Athas et al. 1994).

A stimulator with this stepped voltage waveform will deliver current with some ripple, but that current integrates to the same stimulus charge in the electrode

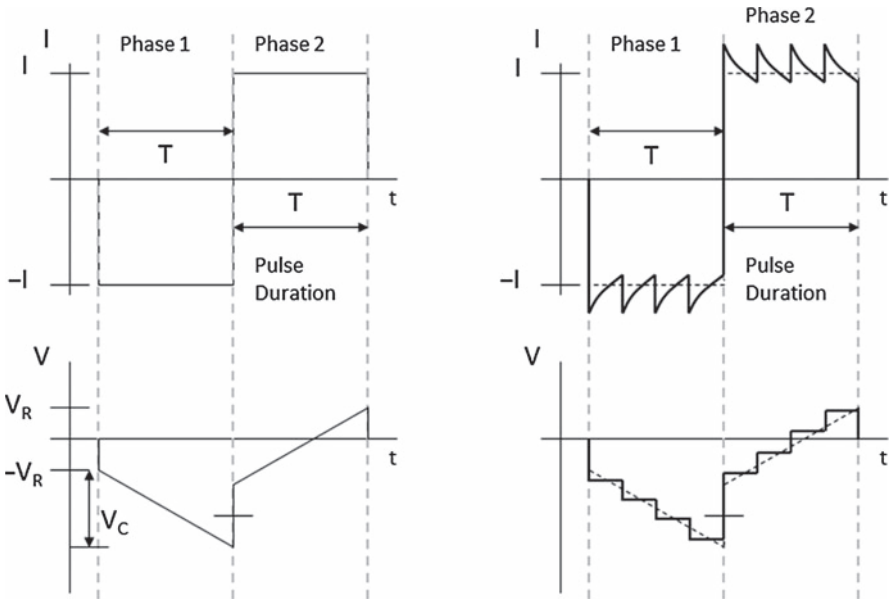

Fig. 10 Electrode current and voltage waveforms, along with approximate waveforms using a voltage step stimulator

capacitance. While this stimulation method can reduce waste power consumption, it requires the series of supply voltages to be generated efficiently. This is achieved by the stimulator architecture that will be explored below.

Example Adiabatic Stimulator Circuit Architecture with Energy Recovery

An example of the stepped, voltage-based stimulator that was described in section "Reducing Sources of Loss" will now be examined. This system's stimulation parameters were informed by a set of acute human retinal stimulation experiments (Rizzo et al. 2003a, b). These trials showed a threshold of approximately 0.8 μC for epiretinal stimulation with pulse widths of several milliseconds. The final parameters implemented in the adiabatic stimulator were 0.678 μC delivered over 5 ms (an average current of 136 μA) into an electrode with resistance 1.15 KΩ and a capacitance of 0.98 μF. The reason for the higher threshold here than in the typical case described in section "Power Consumption in Traditional Neural Stimulators" is that the electrodes in these trials were epiretinal and not tacked down to the retinal surface, so the distance to the neural tissue was greater than what would be expected in a chronic subretinal implant.

A set of voltage steps for the type of stimulation shown in Fig. 10 may be implemented with a bank of power supply capacitors at a range of voltages. Figure 10 shows four voltage steps per stimulation phase, which seems to be a large enough number to get some power reduction benefit, a small enough number to be manageable, and a conveniently round number in binary. It is shown theoretically in Kelly (2004) that using five, four, and three voltage steps per phase consumes 9 %, 15 %, and 32 %, respectively, more than the minimum required I^2R power. A four-step system yields a reasonable power compromise that simplifies the digital state machine design. It is important to point out that this step voltage system is only created once, globally, and that the only circuits repeated for each electrode are the switches to connect to the steps.

Note that the four-step system as shown in Fig. 10 uses eight different voltages in the two phases. This can be simplified in three ways. First, any voltage levels in the positive and negative phases that are near each other can be combined to use only one capacitor. Second, any voltage level that is near ground may be replaced by ground, eliminating a capacitor. Third, the number of first- and second-phase voltage levels that are near each other may be increased by making the capacitive ramp voltages of the two phases overlap more. This is done by reducing the IR voltage relative to the Q/C voltage. Since R, C, and Q are fixed, the current should be reduced and the phase duration increased where allowable. Using these methods allows the eight voltage sources to be simplified down to five. An additional consideration is that some electrodes particularly those using an iridium oxide film surface (sputtered iridium oxide film, SIROF, or activated iridium oxide film, AIROF) have increased cathodic pulse charge capacity if a small anodic bias is used (Beebe and Rose 1988).

A DC voltage on an electrode may cause some concern, but at a modest anodic bias, the leakage current is low enough to be supported by noninjurious reactions with the fluid buffer. This biasing is commonly done with iridium oxide electrodes and is generously considered to be a safe practice (McCreery et al. 1990), though it has not been used in human trials. This anodic offset eases the requirements on the power converter by balancing the demands between the positive and negative phases of the power secondary coil voltage. In other words, instead of creating four negative supplies and one positive supply, the power converter creates three negative and two positive supplies. One particular arrangement of power supply capacitor voltages and resulting electrode currents is shown in Fig. 11.

The anodic bias is equal to one voltage step, so the electrodes are biased to voltage V_{Cp1}. As shown in Fig. 11, the electrode is switched from V_{Cp1} first to V_{mid} (the electrode current return or counter electrode); then to V_{Cn1}, V_{Cn2}, and V_{Cn3} to generate the negative current; and then to V_{Cn1}, V_{mid}, V_{Cp1}, and V_{Cp2} to generate the positive current. Electrodes are drawn back to V_{Cp1} between stimulus pulses by a very weak (200 nA) current source. Notice that voltages V_{Cn1} and V_{mid} are visited in both the negative and positive directions. While V_{mid} is a direct connection to the circuit midpoint (in this case, created by dual half-wave rectifiers), voltage V_{Cn1} is a supply capacitor, which is discharged slightly when supplying negative current to the electrode and recharged slightly when supplying positive current. Thus, the

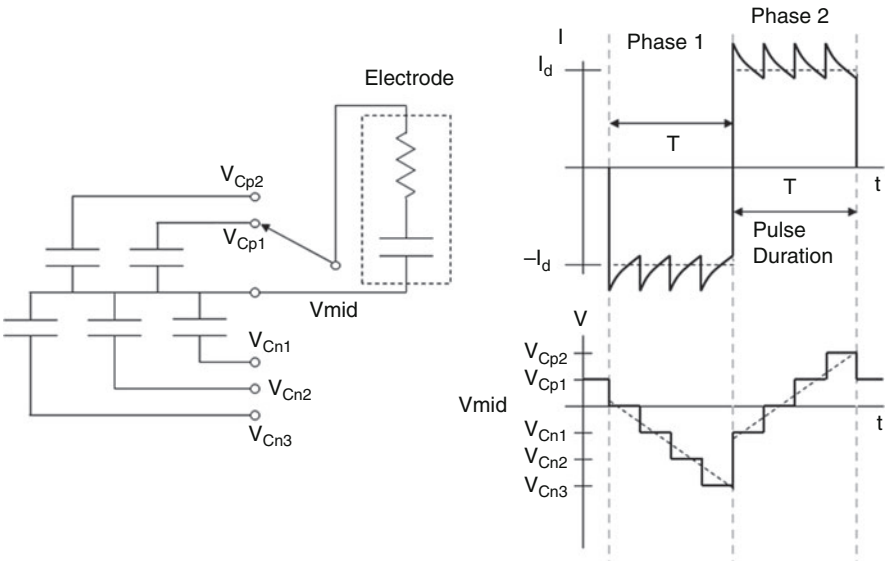

Fig. 11 Architecture of a four-step, five-capacitor voltage step stimulator with one-step anodic bias and approximate current and voltage waveforms

stimulation system is recovering energy from the electrodes to this supply capacitor during the second phase of the stimulation.

Proof-of-Concept Experiments

To test the idea presented above, an AIROF-coated electrode in physiological saline was driven by an arbitrary voltage waveform generator first in the optimal step-ramp pattern described in section "Reducing Excess Voltage Drops" and Fig. 8, then in the stepped pattern described in this section, and in Fig. 11. A simple current sense amplifier served as the return path, sensing current through the electrode. The results of these experiments are shown in Fig. 12. The left side shows the step-ramp voltage waveform and resulting current. Note the consistency in the current plot which shows overlaid data from five different measurements. Note also that the current waveform is not square. The initial peak in the

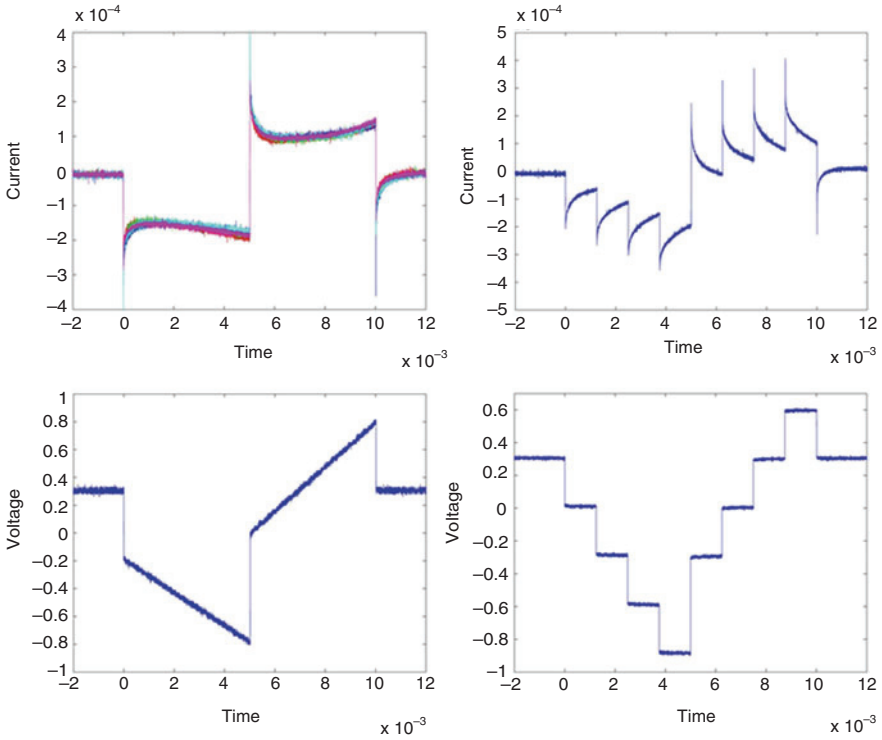

Fig. 12 Bench electrode drive test results with an arbitrary voltage waveform generator (*bottom graphs*) and the resulting current through the electrodes (*top graphs*). The left side shows an ideal step-ramp voltage drive, while the right side shows a four-step stimulating voltage drive

current is due to the nonidealities of the electrode impedance. The right side of Fig. 12 shows the four-step voltage system described in this section and its resulting current waveform.

Single-Coil Multivoltage Power Supply for Neural Stimulation

The capacitive voltage supplies described above may be created by means of a controlled synchronous rectifier from a single alternating voltage on a secondary coil, which receives wirelessly transmitted power via inductive coupling. Alternating current through an external coil creates an alternating magnetic field, which is in turn coupled by an implanted coil, creating an alternating voltage. The rectification step must be done efficiently for the stimulator system as a whole to save any power. In addition, because of the small power budget (~10 mW) and size restrictions for a retinal implant or for some other implanted medical devices, DC-DC switching power converters are usually not a viable option. In this system, the overall power supply for control circuitry on the chip is generated by two simple half-wave rectifiers, using Schottky diodes.

Inductive Power Transmission

Power is delivered to the implant chip via an inductive link operating at 125 KHz. Primary (external) and secondary (implanted) coils are hand-wound on plastic forms. The primary coil, shown on the left in Fig. 13, consists of 45 turns of

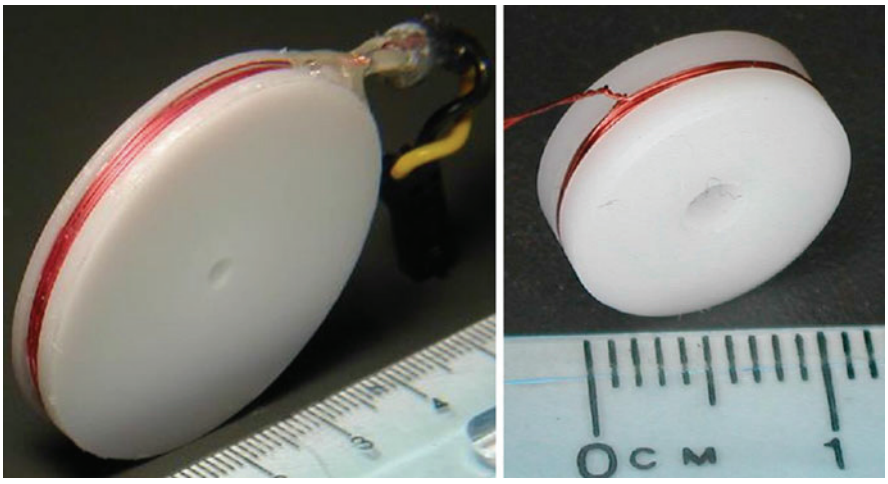

Fig. 13 The primary (*left*) and secondary (*right*) power telemetry coils used in the proof-of-concept wireless adiabatic stimulation system

30 AWG magnet wire with a mean diameter of 37 mm and an inductance of 153 μH. The secondary coil, shown on the left in Fig. 13, consists of 60 turns of 36 AWG wire with a mean diameter of 11 mm and an inductance of 58 μH. The primary is driven by a class E power amplifier, and the secondary is held 15 mm from the primary in a nonconductive plastic test jig. The primary drive current is set so that the voltage at the secondary coil yields ±1.75 V power supplies after the dual half-wave Schottky rectifiers.

Synchronous Rectifier Chip Architecture

The controlled synchronous rectifier forms the core of this design, taking the AC voltage from the secondary coil and creating five separate voltage supplies. The rectifier architecture is shown in Fig. 14. On the left, a transistor threshold-based reference is used and is buffered for the chip's PMOS and NMOS bias voltages (pbias and nbias). The rectifier reference voltages are then derived in the circuit labeled Vref, which feeds a constant current through a string of on-chip resistors. These reference voltages determine the voltage to which the supply capacitors will be charged. The reference voltages are buffered and sent to the column of clocked comparators near the middle of Fig. 14, where the supply capacitor voltages are compared to the references on every cycle. Below the clocked comparators, the clock generation circuitry is shown. A clock is extracted from the 125 KHz coil voltage, labeled AC throughout the figure, and turned into a sequence of clock edges for the comparators. The comparator outputs feed into the control circuitry, which, in part, determines which supply capacitor will be monitored by the continuous comparator. This comparator turns on the appropriate rectifier switch, via the control circuitry, when the AC voltage exceeds the monitored capacitor voltage. Finally, a power-on reset circuit ensures that all circuits initialize to a known state.

Rectifier Reference Voltages

The controlled synchronous rectifier works by turning on a rectifier switch between the secondary coil and one supply capacitor, charging the capacitor up to a specified reference voltage. The reference voltages are created by driving DC current through a string of on-chip polysilicon resistors. The current is determined by a reference based on the transistor threshold voltage (V_T reference) and three off-chip selector switches to correct for process variation. This reference circuit is shown in Fig. 15. The voltage steps are typically set to between 0.12 and 0.25 V, but the full range of the supplies is from 0.07 to 0.33 V. Output voltages are shown in Fig. 16, with the reference voltage circuit input bits being stepped up in value. This voltage selectability allows the stimulator to account for a wide range of electrode impedances or tissue stimulation thresholds. In a tissue stimulator for human use, even more flexibility may be required.

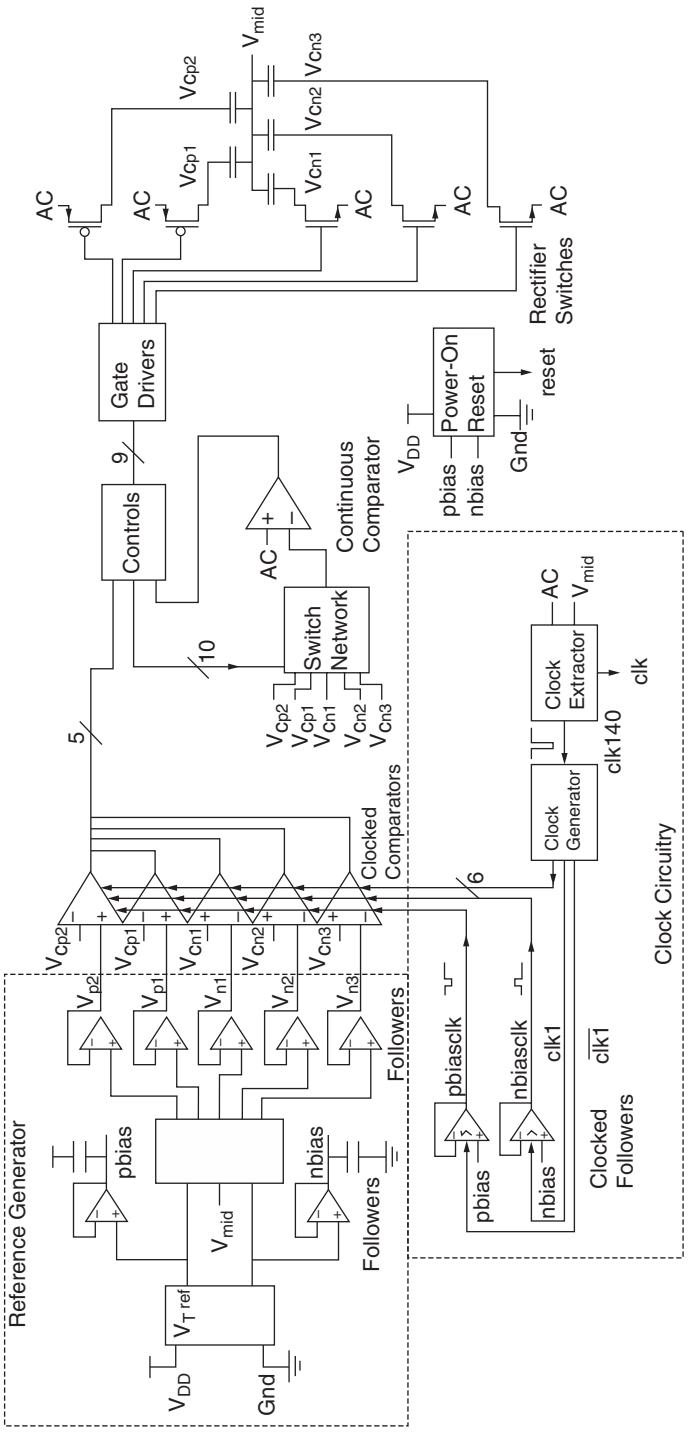

Fig. 14 Block diagram architecture of the synchronous rectifier chip. The capacitor voltages are compared to the generated reference voltages (*upper left*). Any capacitor needing charge is connected to the AC supply when the AC voltage exceeds that capacitor's voltage (*center*, *upper right*)

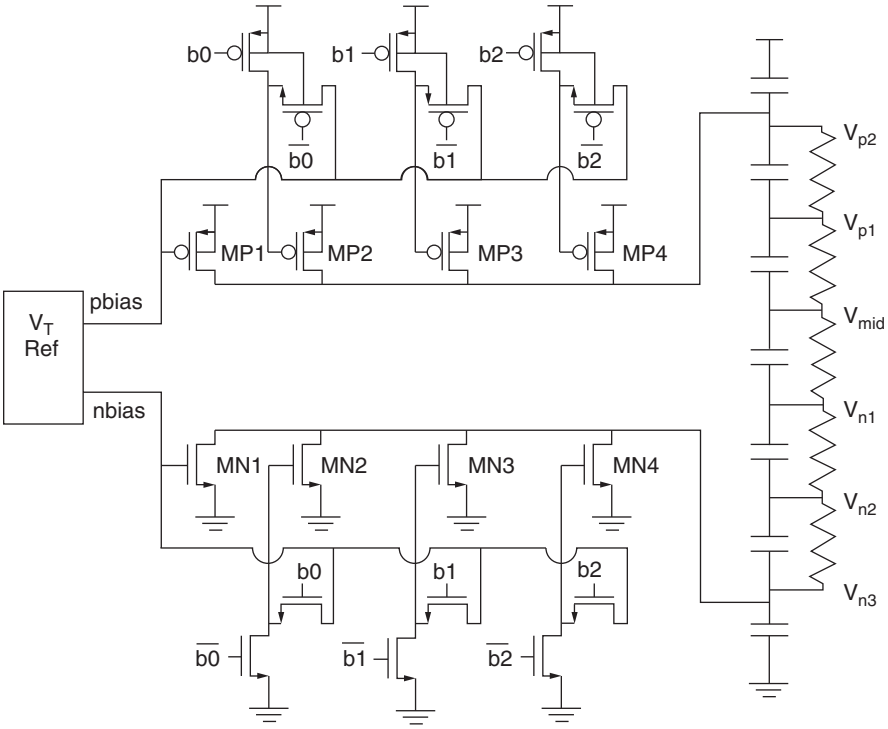

Fig. 15 Reference voltage generator. A V_T-based reference generates selectable currents which run through a string of polysilicon resistors to set up voltage step references

Clocked Comparators

Since the supply capacitor voltages and the buffered reference voltages are DC values, they are compared in a very sensitive clocked comparator, shown in Fig. 17. The core of this circuit is the cross-coupled inverter pair formed by MN1, MP1, MN2, and MP2. The circuit works by allowing the inputs to take control of the weakened inverter pair, after which the inverter pair is powered to latch the result. Specifically, each inverter has two connections to each power supply: (1) a constant weak one, through transistors MP3, MP4, MN3, and MN4, connected to pbias and nbias, and (2) a clocked strong one, through transistors MP5, MP6, MN5, and MN6, connected to pCLK and nCLK. During a voltage comparison, the cross-coupled inverters are first weakened (pCLK and nCLK turned off). Next, the dual differential pairs made up of MN7 and MN8 and MP7 and MP8 are powered (pbiasCLK and nbiasCLK turned on), the passgates from the differential pairs to the cross-coupled inverters are enabled (CLK1 on), and the passgates to the output latch are disabled (CLK2 off). The differential pairs control the inverter pair based on the capacitor and reference voltages, and then the clocks are reset in the same sequence. The cross-coupled pair engages first to latch the comparison (pCLK, nCLK), then the

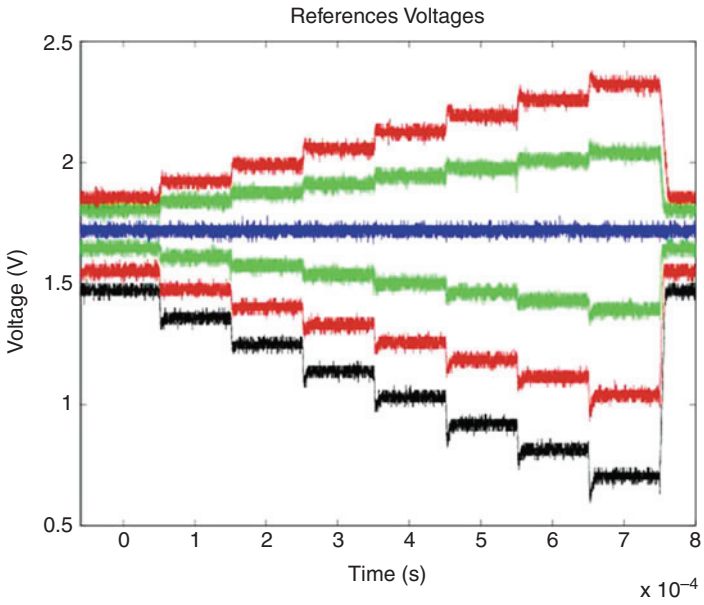

Fig. 16 Reference voltage circuit test results. This plot shows the eight voltage levels of the five reference channels. The center line is Vmid; lines above Vmid are reference voltages Vp1 and Vp2, respectively; and lines below are Vn1, Vn2, and Vn3

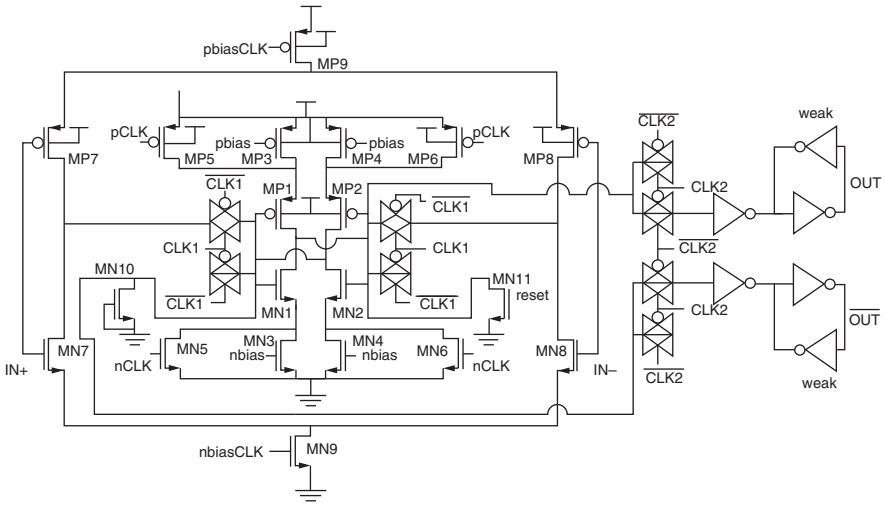

Fig. 17 Clocked comparator. The cross-coupled inverter pair formed by MP1, MP2, MN1, and MN2 latches the difference between inputs IN+ and IN−. The inverter pair is weakened during sampling by turning off pCLK and nCLK

differential pairs turn off, the input passgates disable, and the output passgates enable (pbiasCLK, nbiasCLK, CLK1, CLK2). The result is a sensitive, low-power comparator. In the example case, the comparator consumed 11 pC of charge from a 3.5 V supply in one 140 ns comparison. At 125 KHz, this amounts to an average of 4.8 μW, and there were five comparators in the design, one for each supply capacitor.

Continuous Comparator

The timing for turning on the rectifier switches to charge the supply capacitors is determined by a continuous comparator that monitors the AC coil voltage and a selected capacitor. This is shown in the middle of the block diagram in Fig. 14. This comparator needs to be fast enough to follow the rising edge of the 125 KHz voltage on the secondary power coil and turn on the rectifier switch with negligible delay, yet consume very little power. This is accomplished by using a predictive front end, slightly modified from that described by MeVay and Sarpeshkar in (MeVay and Sarpeshkar 2003). This comparator architecture, shown in Fig. 18, uses a self-biased Bazes' very wide common-mode range differential amplifier (VCDA) (Bazes 1991) for rail-to-rail comparator operation at only 54 μW, but adds the predictive front end to shift the DC comparison voltage based on the slope of the AC voltage. The

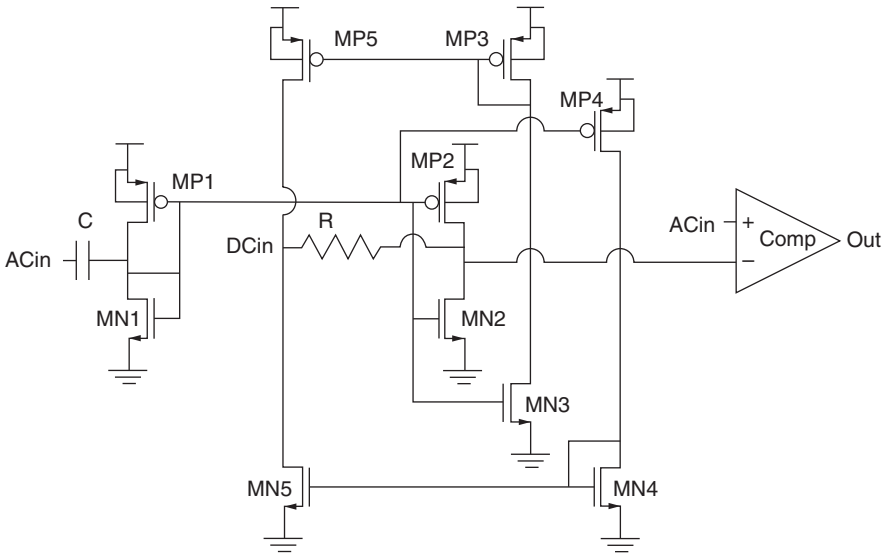

Fig. 18 Predictive comparator front end. The AC input injects current into the mirror, which is drawn through the resistor connected to the DC input. The AC voltage is compared to the DC voltage minus a component proportional to the slope of the AC. The mirrors created by MN3, MP3, MN4, MP4, MN5, and MP5 form a first-order current cancellation circuit

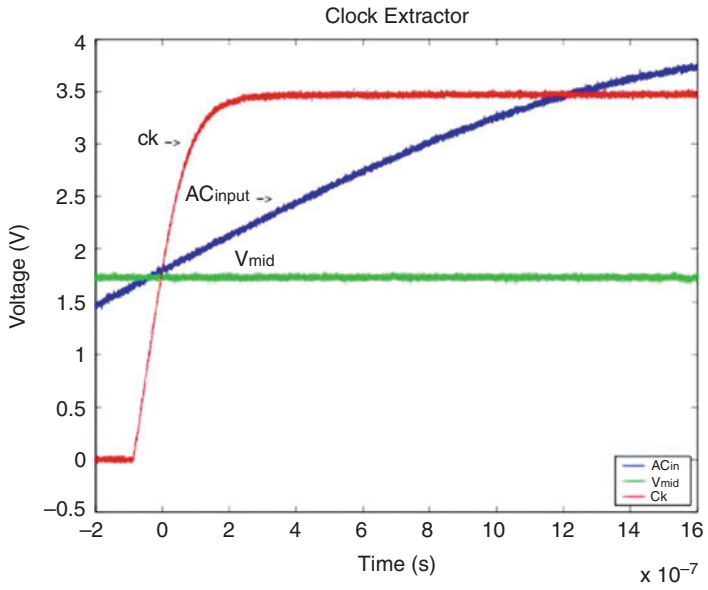

Fig. 19 Continuous comparator with predictive front end, extracting the 125 KHz system clock from the AC coil voltage

capacitor on the left of the figure injects into the current mirrors a current proportional to the slope of the AC voltage. This current is mirrored via either MP1/MP2 or MN1/MN2 into the resistor connected to the DC voltage (in this case the supply capacitor), and the modified voltage is used for the comparison. For example, if the AC voltage is rising, current is injected into MN1, and MN2 pulls current out of the resistor. This reduces the voltage at the input of the comparator to a value lower than the actual DC voltage, causing the comparator to begin to change state earlier. If the predictive time shift can be matched to the comparator delay, a low-power comparator can be made to have a very small delay. The other mirrors in Fig. 18, with transistors numbered 3 through 5, are added to give first-order cancellation of the resistive current at the DC voltage node. The predictive comparator used here in a synchronous rectifier role has a very low power-delay product in a low-power application where losses need to be eliminated. A faster traditional comparator would consume too much current, and a slower comparator would cause too much turn-on delay, increasing losses in the rectifier switches. A version of this comparator is used to extract the 125 KHz clock from the AC coil voltage, and a sample clock comparison is shown in Fig. 19.

System Implementation and Testing

The low-power stimulator chip shown in Fig. 20 was fabricated in a CMOS process and tested in a nonconductive test jig with a wireless inductive power supply and preprogrammed data. The system drove a set of sputtered iridium oxide (SIROF)

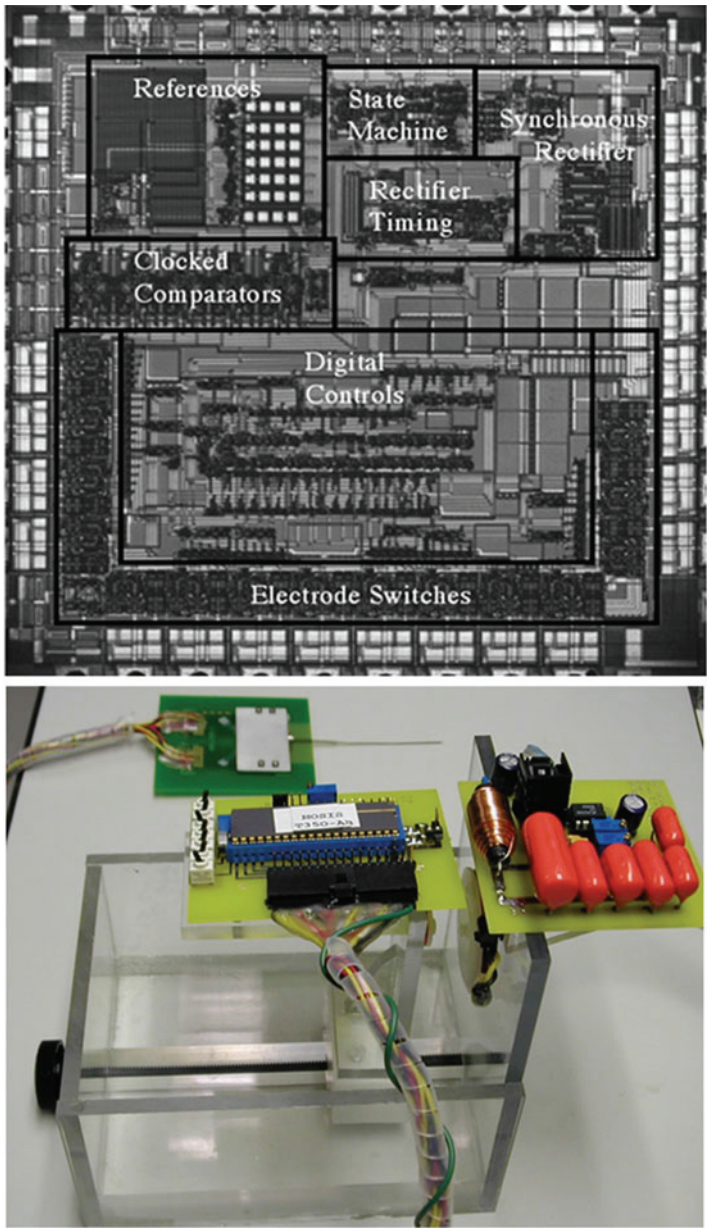

Fig. 20 At the *left*, the adiabatic stimulator chip and, at the *right*, the full wireless system tested in a nonconductive test jig, connected to SIROF electrodes (*background*)

electrodes in a buffered saline solution, with a large separate return electrode. Electrode current was measured with a small series resistor and an instrumentation amplifier. The measured electrode current and voltage waveforms are shown in

Fig. 21. Note the similarities between these waveforms, the predicted waveforms in Fig. 11, and the measured waveforms in Fig. 12. The voltage waveform is very close to the desired waveform, while the current has slightly higher peaks than desired for optimal efficiency. The current in Fig. 21 integrates to 0.678 μC per phase, close to the measured human epiretinal perceptual threshold of 0.8 μC (Rizzo et al. 2003a). Power consumption for the entire system was calculated directly from the secondary coil voltage and current, measured by an instrumentation amplifier. This gave the total power consumed downstream from the coil. The dissipation of the coil was then added to that value. These values account for all of the power delivered to the secondary coil by the magnetic field. They were taken when driving no electrodes and again when driving 15 electrodes.

The data in Table 1 show that the total power (including secondary coil losses) required to drive 0.678 μC into each of 15 electrodes at 100 Hz frame rate is 2.22 mW. Since the system consumes 338 μW of power with no electrodes driven, the cost of electrode stimulation, including *all* system inefficiencies, is 1.88 mW or 125 μW per electrode. A very aggressive traditional current source design using the same ±1.75 V supplies created with an efficient 0.25 V Schottky diode rectifier, delivering the same charge in the same time, will use 271 μW per electrode, not

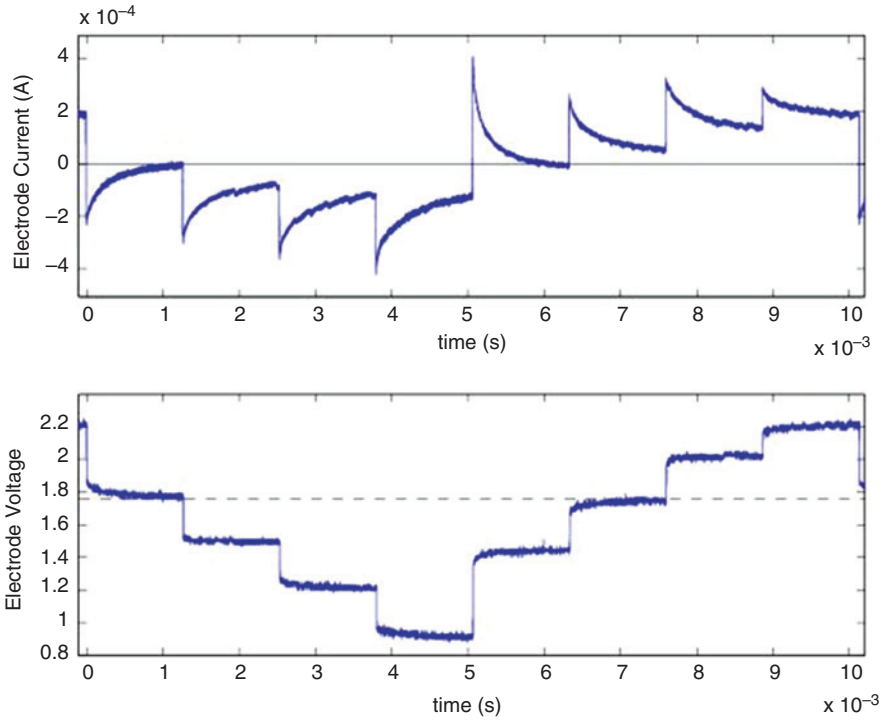

Fig. 21 Measured electrode current and voltage waveforms. Compare the current and voltage waveforms to those predicted in Fig. 11. Voltage waveforms here are with respect to the chip ground, not V_{mid} (1.75 V)

including overhead control power. This design represents a 53 % power savings over such an extremely aggressive current source design. A more typical, yet still aggressive, current source stimulator might use ±2.5 V supplies, consuming 373 μW per electrode, nearly three times the power consumption of this design. Most current source stimulators use much higher voltages than this in an attempt to improve current source output impedance and to hedge against future voltage compliance requirements that arise from impedance variations or stimulus threshold charge or current variations. The architecture presented here includes programmable voltage supply levels which can be designed with a broader range to give the minimum voltage required to drive the threshold charge into the electrodes, while reserving the capability to increase the voltage supplies at a later time to drive more charge or larger electrode impedances.

For reference, it can be calculated from Eq. 7 that the theoretical minimum power consumption within electrodes receiving this charge stimulation is 21.2 μW. The power delivered to the electrodes by our system was calculated from the product of the electrode voltage and current and was found to be 49 μW per electrode. Table 2 shows a comparison of all of these values. Let us consider the losses in this system, the difference between the theoretical 21.2 μW measured 49 μW into the electrode and measured 125 μW per electrode for the whole system. The 49 μW measured electrode power includes several inefficiencies, including the current peaking from using voltage steps as well as nonidealities in the electrode impedance. The 125 μW measurement is more obvious, as it includes losses in the rectifier switches and increased coil losses. To further reduce this power and increase efficiency, a voltage-based stimulation system could be designed which tracks the electrode voltage, as shown in the bench tests in Fig. 12.

Table 1 Stimulator system power consumption. Power consumed while driving 15 electrodes is compared to power in the standby state, driving no electrodes

	15 Electrodes		No electrodes	
	Mean	St. dev.	Mean	St. dev.
Coil power	44.4 μW	14.1 μW	2.79 μW	0.11 μW
Electronics power	2.18 mW	0.691 mW	335 μW	20.1 μW
Total power	2.22 mW	0.703 mW	338 μW	20.2 μW

Table 2 Comparison of power consumed per electrode. The most direct comparison is net power during stimulation, shown in bold

Theoretical	Minimum possible power	21.2 μW
This system	Measured power into electrode	49 μW
This system	**Net power during stimulation (not including overhead)**	**125 μW**
This system	Gross power during stimulation (including all overhead)	148 μW
Aggressive current source system	**Net power during stimulation (not including overhead)**	**271 μW**
Typical current source system	**Net power during stimulation (not including overhead)**	**373 μW**

Conclusion

The stimulation system presented here realizes power savings of 53 % over an extremely aggressive traditional current source design and 66 % or more over commonly used designs. It does this by using a voltage-based design, which has efficiency benefits over a current source design but is generally avoided in neural and other tissue stimulators. This efficiency requires trade-offs, resulting in decreased current precision and increased complexity of the power management system. A practical implementation of this system will require careful control of the step voltages and should include the ability to control the steps via telemetered data or by a current feedback system on-chip. In a medical application, the architecture described here would require additional safeguards to measure and limit total charge delivered, but these safeguards can easily be added, and the power savings of this design justify the increased complexity.

A number of improvements can be made to a future design. First, a stepped voltage system such as that described here could use simple current sources instead of switches to connect the electrodes to the steps. This would limit the peak current to the electrodes and keep it closer to the constant current waveform. In addition, as neural stimulators, in particular retinal prostheses, implement more and more stimulating electrodes, the size of each electrode will likely decrease, with each electrode targeting a smaller number of nerve cells, and greater charge-delivery precision will be required. The simple current sources can take advantage of the power savings of the multiple voltage step architecture while more precisely controlling the total charge delivered to the tissue. Second, if the resistance of electrodes embedded in tissue increases (Cogan 2006) so that the RC product significantly exceeds the maximum desirable stimulation pulse width (5 ms in this example design, often up to 8 ms in clinical designs), this stepped design will prove less effective. In this case, the electrode voltage profile under constant current stimulation looks more square, and a current source could provide this stimulus from one supply at the minimum required voltage. A network of voltage supplies can be used to drive different electrodes with different impedances or require different threshold charge levels. These circuit solutions may increase device complexity, but the power savings realized can lead to size, safety, and longevity improvements in implanted tissue stimulators, especially those with large numbers of electrodes, such as retinal prostheses for the blind.

References

Athas WC, Koller JG, Svensson LJ (1994) An energy-efficient CMOS line driver using adiabatic switching. In: Proceedings of the 4th great lakes symposium. VLSI Design Automation of High Performance VLSI Systems, pp 196–199

Bazes M (1991) Two novel fully complementary self-biased CMOS differential amplifiers. IEEE J Solid-State Circ 26(2):165–168

Beebe X, Rose TL (1988) Charge injection limits of activated iridium oxide electrodes with 0.2 ms pulses in bicarbonate buffered saline. IEEE Trans Biomed Eng 35(6):494–495

Chen K, Lo Y, Yang Z, Weiland J, Humayun MS, Liu W (2013) A system verification platform for high-density epiretinal prostheses. IEEE Trans Biomed Circ Syst 7(3):326–337
Cogan S (2006) In vivo and in vitro differences in the charge-injection and electrochemical properties of iridium oxide electrodes. In: Proceedings of the IEEE international conference of the Engineering in Medicine and Biology Society, pp 882–885
Dickinson AG, Denker JS (1994) Adiabatic dynamic logic. In: Proceedings of the IEEE Custom Integrated Circuits Conference, pp 282–285
Fried SI, Hsueh HA, Werblin FS (2006) A method for generating precise temporal patterns of retinal spiking using prosthetic stimulation. J Neurophysiol 95(2):970–978
Gorman PH, Mortimer JT (1983) The effect of stimulus parameters on the recruitment characteristics of direct nerve stimulation. IEEE Trans Biomed Eng 30:407–414
Gosalia K, Weiland J, Humayun M, Lazzi G (2004) Thermal evaluation in the human eye and head due to the operation of a retinal prosthesis. IEEE Trans Biomed Eng 51(8):1469–1477
Hallum LE, Dagnelie G, Suaning GJ, Lovell NH (2007) Simulating auditory and visual sensorineural prostheses: a comparative review. J Neural Eng 4:S58–S71
Humayun MS, Dorn JD, da Cruz L, Dagnelie G, Sahel J-A, Stanga PE, Cideciyan AV, Duncan JL, Eliott D, Filley E, Ho AC, Santos A, Safran AB, Arditi A, Del Priore LV, Greenberg RJ (2012) Interim results from the international trial of Second Sight's visual prosthesis. Am Acad Ophthalmol 119(4):779–788
Jensen RJ, Ziv OR, Rizzo JF (2005) Responses of rabbit retinal ganglion cells to electrical stimulation with an epiretinal electrode. J Neural Eng 2(1):S16–S21
Jia H, Cheng X, Wang X, Kumar P, Shen ZJ (2008) A novel monolithic self-synchronized rectifier. In: Proceedings of the IEEE Applied Power Electronics Conference and Exhibition, pp 907–912
Kelly SK (2004) A system for efficient neural stimulation with energy recovery. Dept. Electrical Eng. and Computer Science, Massachusetts Institute of Technology, Cambridge, MA
Kelly SK, Wyatt JL (2011) A power-efficient neural tissue stimulator with energy recovery. IEEE Trans Biomed Circ Syst 5(1):20–29
Kelly SK, Shire DB, Chen J, Doyle P, Gingerich MD, Cogan SF, Drohan W, Behan S, Theogarajan L, Wyatt JL, Rizzo JF (2011) A hermetic wireless subretinal neurostimulator for vision prostheses. IEEE Trans Biomed Eng 58(11):3197–3205
Kelly SK, Shire DB, Chen J, Gingerich MD, Cogan SF, Drohan WA, Ellersick W, Krishnan A, Behan S, Wyatt JL, Rizzo JF (2013) Developments on the Boston 256-channel retinal implant. In: IEEE international conference on Multimedia and Expo, MAP4VIP workshop, pp 1–6
Lapicque L (1907) Recherches quantitatives sur l'excitation electrique des nerfs traites comme une polarization. J Physiol Paris 9:622–635
McCreery DB, Agnew WF, Yuen TGH, Bullara L (1990) Charge density and charge per phase as cofactors in neural injury induced by electrical stimulation. IEEE Trans Biomed Eng 37 (10):996–1001
Merrill DR (2010) The electrochemistry of charge injection at the electrode/tissue interface. Implantable Neural Prostheses 2: Techniques and Engineering Approaches. In: Zhou DD, Greenbaum E (eds). Springer
MeVay ACH, Sarpeshkar R (2003) Predictive comparators with adaptive control. IEEE Trans Circ Syst II Analog Digit Sig Process 50(9):579–588
Pan H, Liang YC, Oruganti R (1999) Design of a smart power synchronous rectifier. IEEE Trans Power Electron 14(2):308–315
Rizzo JF, Wyatt JL, Loewenstein J, Kelly SK, Shire DB (2003a) Methods for acute electrical stimulation of retina with microelectrode arrays and measurement of perceptual thresholds in humans. Invest Ophthalmol Vis Sci 44(12):5355–5361
Rizzo JF, Wyatt JL, Loewenstein J, Kelly SK, Shire DB (2003b) Perceptual efficacy of electrical stimulation of human retina with a microelectrode array during short-term surgical trials. Investig Ophthalmol Vis Sci 44(12):5362–5369
Testerman RL, Rise MT, Stypulkowski PH (2006) Electrical stimulation as therapy for neurological disorders. IEEE Eng Med Biol Mag 25:74–78
Weiss TF (1996) Cellular biophysics, vol. 2: electrical properties. MIT Press, Cambridge, MA.